SESSION 11 – TAPA III
Signal Processing

Friday, June 18, 10:20 a.m.
Chairpersons: K. Roy, Purdue University
K. Kobayashi, Kyoto University

11.1 — 10:20 a.m.
VLSI Processor for Reliable Stereo Matching Based on Window-Parallel Logic-in-Memory Architecture, M. Hariyama and M. Kameyama, Tohoku University, Sendai, Japan

This paper presents a VLSI processor for reliable stereo matching between images by selecting a desirable window size. A degree of parallelism between pixels in a window changes depending on its window size, while a degree of parallelism between windows is predetermined by the input-image size. Based on this consideration, a window-parallel and pixel-serial architecture is proposed to achieve 100% utilization of processing elements(PEs). Its simple interconnection network between memory and PEs also makes it superior to the pixel-parallel-architecture-based VLSI processors.

11.2 — 10:45 a.m.
A 2.8 Gb/s, 32-State, Radix-4 Viterbi Decoder Add-Compare-Select Unit, N. Bruels, E. Sicheneder, M. Loew, A. Schackow, J. Gliese and C. Sauer, Infineon Technologies, Munich, Germany

A 0.13µm CMOS add-compare-select unit (ACSU) is presented allowing for a maximum data rate of 2.8 Gb/s. A modified bit-level pipelining scheme combined with a new state metric representation has been implemented using single-rail DOMINO logic and static CMOS gates. The adaptation of architecture and circuit technique results in a compact energy-efficient design. The 0.5mm2 chip consumes 970mW at 2 Gb/s (VDD = 1.2 V) and 2.2 W at 2.8 Gb/s (VDD = 1.5 V).

11.3 — 11:10 a.m.
A 64-state 2GHz 500Mbps 40mW Viterbi Accelerator in 90nm CMOS, M. Anders, S. Mathew, R. Krishnamurthy and S. Borkar, Intel Corporation, Hillsboro, OR

A 64-state Viterbi accelerator fabricated in 1.2V, 90nm dual-Vt CMOS technology is described for 2GHz operation and fastest reported 500M bps data rate (1Gbps decode for ½ rate codes). Novel radix-4 add-compare-select circuits and low-energy traceback register file techniques enable 40mW total power at 1.2V, 2GHz, and scalability to 5mW at 0.7V, 216MHz (for 802.11a wireless baseband).

11.4 — 11:35 a.m.
A Technique to Build a Secret Key in Integrated Circuits for Identification and Authentication Applications, J.W. Lee, D. Lim, B. Gassend, G.E. Suh, M. van Dijk and S. Devadas, MIT, Cambridge, MA

This paper describes a technique that exploits the statistical delay variations of wires and transistors across ICs to build a secret key unique to each IC. We fabricated a candidate circuit to generate a response based on its delay characteristics. We show that there exists enough delay variation across ICs implementing the proposed circuit to identify individual ICs. Further, the circuit functions reliably over a practical range of environmental variation such as temperature and voltage.

Lunch 12:00 pm